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An Ultra-Low Power Edge Combining BPSK Transmitter

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An Ultra-Low Power Edge Combining BPSK Transmitter

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***Abstract*—There is a growing need in the armed forces for small, low-profile, electronic devices that can easily be concealed and/or worn in clothing. These tiny devices can be worn by warfighters to monitor their health status as well as their location and any other sensor data that is desired. The data would be transmitted to a remote device, but the conventional transmitter would suffer from high power consumption. In this document, we propose two versions of ultra-low power binary phase-shift keying (BPSK) transmitters employing injection locking frequency multiplication for near field (~2m) communication. The power consumption of the proposed transmitters ranges from 90 to 125 µW with the target data rate of 120 kbps. We intend to achieve this by choosing a design that does not require a power-hungry oscillator and employing a power-efficient transmitter architecture. The custom transmitter will be designed by addressing the trade-offs between phase noise performance, output power, and bit-rate for power consumption.**

I. Introduction

As technology advances and transistor size decreases, electronic devices become more compact and mobile. Whether the application for the electronic device is for data collection, storage, processing, or communication, data are passed on from one device to another. To make the data transfer easier, wireless data transmission becomes a critical portion of mobile devices. However, a wireless transceiver, especially a transmitter, dominates the power consumption in a mobile device, which limits the battery operation life.

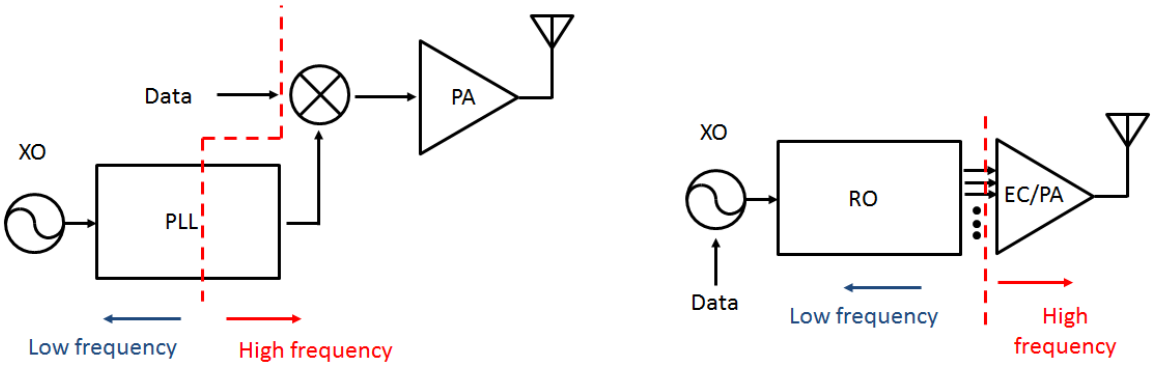
The most widely employed transmitter architectures entail double frequency conversion because of its robust structure and proven performance. However, this architecture suffers from high power consumption largely due to high complexity in system architecture. Particularly, power amplifier (PA) and high-frequency phase locked loop (PLL) lead to high power consumption due to high-frequency accuracy and low phase noise requirements.

Recently, several ultra-low power transceiver architectures have been proposed. By employing simple modulation schemes such as amplitude modulation (AM) or on-off keying (OOK), the complexity of the system reduces, thereby decreasing the power consumption [1], [2], [3]. However, these modulation schemes suffer from noise and bandwidth inefficiency [4]. A frequency-based modulation scheme such as frequency modulation (FM) or frequency shift keying (FSK) also has a simple architecture, which consumes low power, but it is still vulnerable to noise and bandwidth inefficiency. A phase-shift keying (PSK) modulation scheme utilizes phase information, therefore it is less susceptible to noise and also bandwidth efficient compared to FSK. Nevertheless, a conventional BPSK transmitter requires higher order of complexity in the architecture, and therefore requires higher power consumption.

In this document, we propose two versions of transmitters with the advantages of the BPSK modulation, which dissipates less than 150 µW with the data rate of 120 kbps. The target data rate may be pushed up to 1.5 MHz, but a more accurate number will be obtained through measurements. A 120-kbps data rate is targeted for the application in biopotential measurements. The proposed transmitter utilizes the injection-locked frequency multiplication (ILFM) technique as reported in [5]. The output frequency target is 405 MHz, which is a part of the medical implant communication service (MICS) band. The output power target is between -17 and -20 dBm. The proposed transmitter may be used with FSK or OOK modulation and possibly used to meet the MICS standard. However, the purpose of this work is to further demonstrate the BPSK functionality at an ultra-low power level. The proposed transmitter is designed and simulated in cadence with IBM CMOS 65-nm technology.

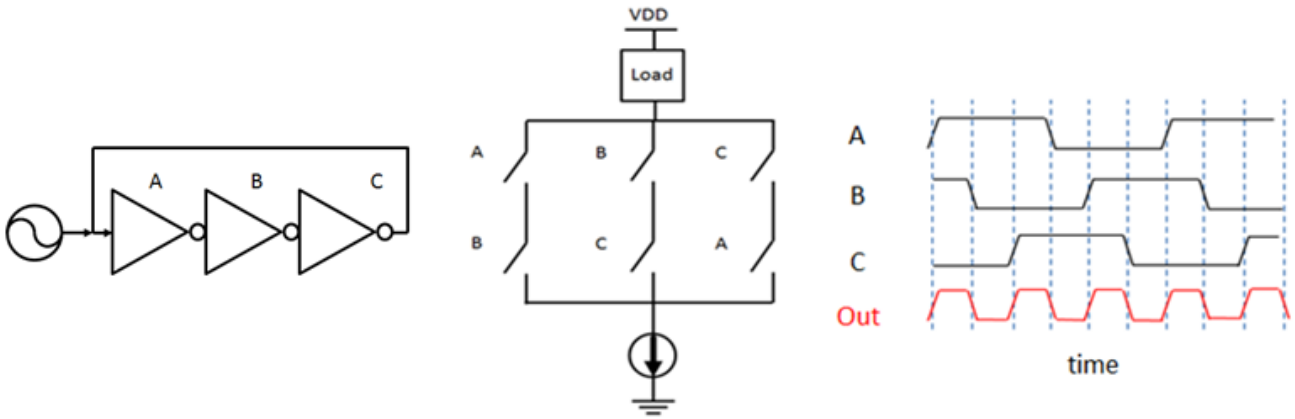
II. Principle of the ILFM

The motivation and the principle of the ILFM are extensively explained in [5]. The major goal of the ILFM is to simplify the transmitter architecture and reduce the number of systems operating in high frequency as depicted in Fig. 1. In Fig. 1 (a), a direct conversion transmitter is depicted, which consists of a crystal oscillator (XO), a PLL, a mixer, and a PA. In this architecture, systems on the right side of the red dotted line operate in high frequency. In Fig. 1(b), a crystal is injection locked to a ring oscillator (RO), and then multiple phase outputs are combined at the last edge combining/power amplifier (EC/PA) stage. With the latter architecture, only the last EC/PA stage is operating in high frequency. Notice, not only the number of systems required is reduced, but also the number of systems operating in high frequency is minimized. Therefore, the power consumption can be reduced. In [5], FSK modulation is implemented by modulating the oscillation frequency of the XO.



(a) (b)

Fig. 1. (a) A conventional direct conversion transmitter architecture. (b) Injection locked frequency multiplication transmitter architecture.



(a) (b) (c)

Fig. 2. (a) Block diagram of the crystal oscillator injection locking injection locking to the ring oscillator.
(b) Block diagram of the edge combining power amplifier. (c) Timing diagram displaying the principle of the edge combining.

In Fig. 2, detailed circuit diagrams as well as timing diagrams are illustrated to explain the principle of edge combining. For simplicity, only three stages of the ring oscillator are shown. With the following architecture, the output can be expressed as

$$\text{Out} = AB+BC+CA \quad (1)$$

Due to the equal delays in the outputs of the RO (A, B, and C) and following the output logic as in (1), the output frequency becomes

$$\text{Fout} = \text{Fxo} \times (\#\text{ of RO stages}). \quad (2)$$

Therefore, increasing the number of RO stages results in a higher output frequency. However, employing a higher number of RO stages also increases the power consumption in the RO stage. In [5], nine RO stages are used with the XO frequency of 44.5 MHz to generate output frequency of 400.5 MHz.

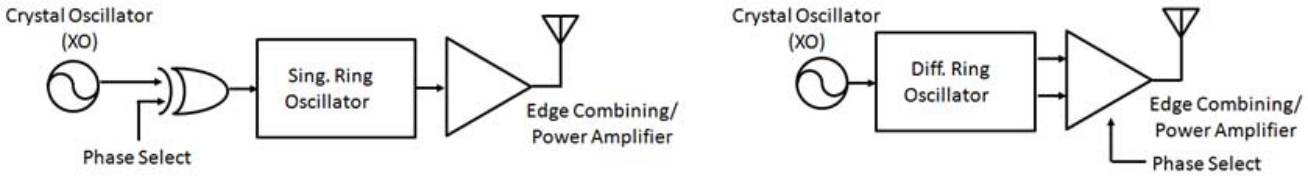
Since this circuit is based on digital logic, if a resistive load is used for EC/PA, then the output becomes a square wave. In order to produce sine wave output, an inductive load can be used to filter out harmonics. An inductive load with a higher quality factor (Q) can suppress the unwanted harmonics better.

III. Proposed BPSK Transmitter

Two versions of ultra-low power BPSK transmitter are proposed in this report as shown in Fig. 3.

A. TX1 with Single ended RO

Fig. 3 (a) presents the first TX version, which resembles the FSK transmitter as reported in [5]. The architecture is utilizing the fact that when two oscillators are injection locked, frequency and phase are both in sync. Without much change from the circuit proposed in [5], an XOR gate is inserted in between an XO and an RO. Therefore, the power consumption is close to the one in [5]. Ideally, the phase of the XO and the RO should be locked, but they may not be in sync despite the frequencies being in sync. Also, there is a transition in phase in the RO stage, which requires extra time for RO to settle to a new phase.



(a) (b)

Fig.3. (a) Block diagram of the single-ended TX1. (b) Block diagram of the semi-differential TX2.

B. TX2 with Differential RO

The next proposed TX utilizes a differential RO as in Fig. 4. In this TX, the semi-differential EC/PA takes differential phase outputs of the RO, but the output is still single ended, and therefore a single-ended antenna can be used. With the current steering phase select controls as shown in Fig. 5, the output becomes

$$\text{Out} = \text{Phase}(AB+BC+CA)+\text{Phase}'(A'B'+B'C'+C'A'). \quad (3)$$

In this configuration, the RO remains undisturbed and there is a clear distinction between in-phase and out-phase signals. However, the usage of differential RO requires extra power consumption. Since only one branch of the EC/PA is on while the other branch is off, there is no extra power consumption from the EC/PA compared to the single-ended TX1.

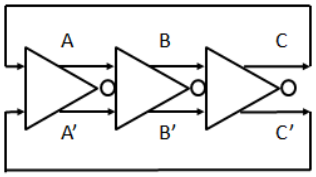


Fig.4. Differential ring.

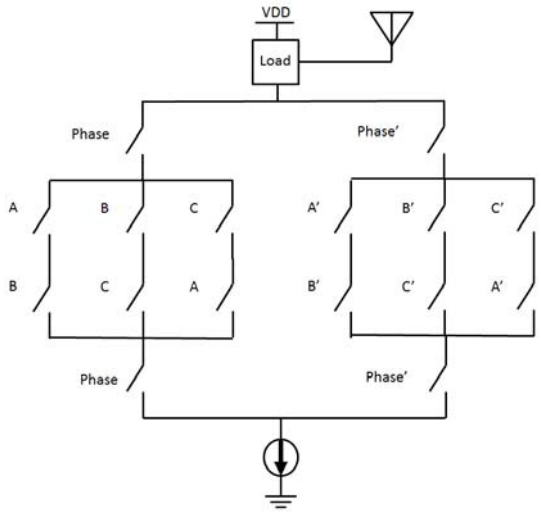


Fig.5. Semi-differential edge combining /power amplifier.

C. Injection Locking

Injection locking is a critical operation in this TX architecture to obtain better phase noise without employing a power-hungry frequency generator. The strength of the injection device determines the injection-locking frequency range. A stronger injection device results in a wider locking range. However, if the injection device becomes too strong, it may override the oscillation behaviour of the RO. In addition, the stronger injection device means additional uneven loading at the injection point, disturbing the phase at the injection node and creating a reference spur. As a rule of thumb, half the strength of the each stage of the RO is recommended for the injection device.

If the XO was injection locking to the RO as shown in Fig. 2 (a), the injection port would have an uneven loading due to the injection device. In [5], a two-stage, multi-point injection is proposed to reduce reference spur and obtain better phase noise. However, this topology still suffers from uneven loading at different nodes. Instead of using a two-stage, multi-point injection, we propose a one-stage injection arranged as in Fig. 6. In this configuration, each output node has an equal loading, which results in an even output phase. The injection scheme in Fig. 6 can be implemented in a differential RO as well.

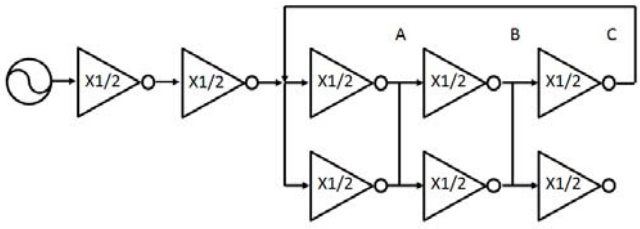


Fig.6. Even-loading, one-stage injection locking in a single-ended representation.

IV. Simulation Results

The simulation was performed in cadence with IBM CMOS 65-nm technology. A 1-V supply voltage is used to lower the power consumption. A 45-MHz XO with nine-stages RO is used to produce a 405-MHz output. Load is an integral part of the system performance, and the output power, maximum data rate, phase noise, and spur level depend on the loading condition. For fair comparison, a 220-nH off-chip inductor with a corresponding matching network is used for

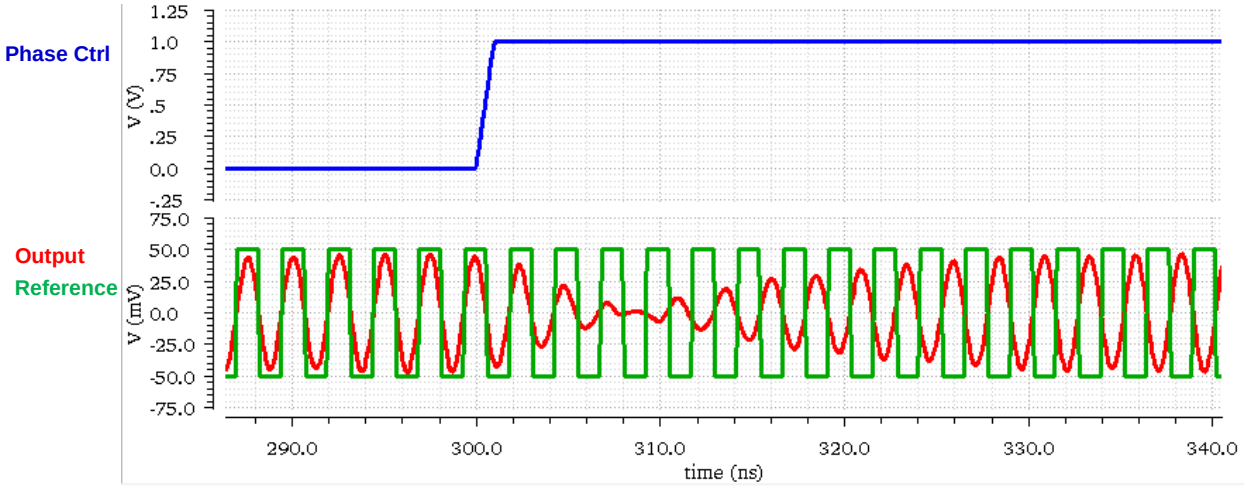


Fig.7. Transient simulation of TX2.

TABLE 1
Ultra-low power transmitter performance summary.

	[1]	[2]	[3]	[5]	TX1	TX2
Power Dissipation	3.8mW/ 9.1mW	700µW/ 1.12 mW	400µW	90µW	90µW	125µW
Pout	-11.4dBm/ -2.2dBm	140µW/ 320µW	-60dBm	-17dBm	-18.8dBm	-19.5dBm
Frequency	916.5M	1.95G/ 2.38G	400M	400M	405M	405M
Energy per bit	3.8nJ/bit 9.1nJ/bit	2.3nJ/bit	1.2nJ/bit	0.45nJ/bit	0.75nJ/bit	1.04nJ/bit
Data Rate	1Mbps	300 kbps/ 1Mbps	120 kbps	200 kbps	120 kbps	120kbps
Process	180nm	130nm		130nm	65nm	65nm
Modulation	OOK	OOK	MSK	BFSK	BPSK	BPSK

simulation to test three proposed transmitters. In practice, practical matching components need to be figured out through trial and error.

In Fig. 7, a transient simulation of TX2 is shown. As the phase select signal changes, the output phase changes accordingly. The settling time for TX1 is 160 ns, while the settling time for TX2 is 30 ns. Extra settling time is required for TX1, since the RO needs to settle to a new phase. In either case, fast settling time is achieved, since no feedback is employed. Assuming the maximum desired data rate is 1.5 MHz, the settling time of the proposed transmitters should not be an issue.

In Table 1, the performances of various ultra-low power transmitters are listed. It is unfair to compare only one parameter. Instead, all parameters, including output power, operating frequency, data rate, and modulation schemes need to be taken into consideration, in conjunction, for fair comparison. Regardless, the proposed transmitters consume relatively lower power compared to others. The TX in [5] stands out the most, with the lowest power consumption and the lowest energy per bit. Obviously, the energy per bit depends on the data rate. For the proposed transmitters, a 120-kbps data rate is used for future application on four channel body-sensor networks, even though the transmitters may operate up to 1.5 Mbps without much added power consumption. Again, the maximum data rate may depend on the loading condition as well. The total power consumption includes 15 µW of power consumption from the XO.

Comparing the TX in [5] with the proposed BPSK transmitters, BPSK can double the spectral efficiency compared to BFSK. Also, BPSK requires less output power than BFSK to obtain the same signal noise ratio (SNR), since information stored in phase is less affected by the noise compared to the information stored in frequency.

Fig.8 presents spectrum of the output of the TX2 with and without the injection locking. With the injection locking, the

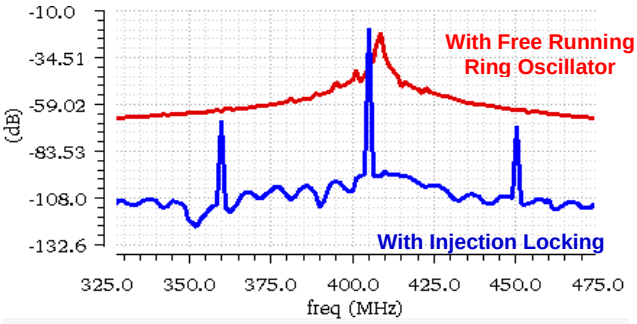


Fig.8. Output spectrum with and without the injection locking for TX2.

phase noise improves over 73 dB. Also, the carrier to spur rejection is 48 dB. Again, these numbers depend on the loading condition, and an accurate number has to be found through test measurements.

V. Conclusion

New BPSK transmitter architectures based on an injection-locking frequency multiplication technique are reported in this document. These ultra-low power transmitters consume 90 to 125 µW. TX1 dissipates the least amount of power, but at the cost of higher settling time compared to the other version and at the risk of unstable RO operation. Nevertheless, both proposed transmitters may be used for short-range (<2 m) communication with the advantages of the BPSK modulation. The design is currently waiting to be sent for fabrication and measured in the future.

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14. ABSTRACT

There is a growing need in the armed forces for small, low-profile electronic devices that can easily be concealed and/or worn in clothing. These tiny devices can be worn by warfighters to monitor their health status as well as their location and any other sensor data that are desired. The data would be transmitted to a remote device, but the conventional transmitter suffers from high power consumption. In this paper, we propose two versions of ultra-low power binary phase-shift keying (BPSK) transmitters employing injection-locking frequency multiplication for near field (~2 m) communication. The power consumption of the proposed transmitters is ranges from 90 to 125 μW with the target data rate of 120 kbps. We intend to achieve this by choosing a design that does not require a power-hungry oscillator and employing a power-efficient transmitter architecture. The custom transmitter will be designed by addressing the trade-offs between phase noise performance, output power, and the bit-rate for power consumption.

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